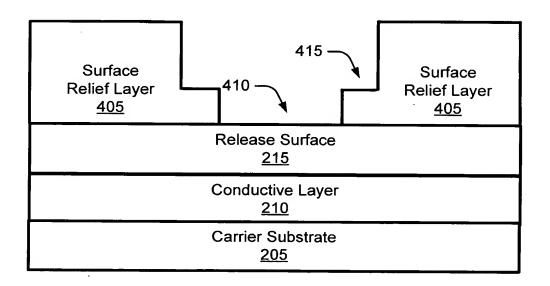


Fig. 4



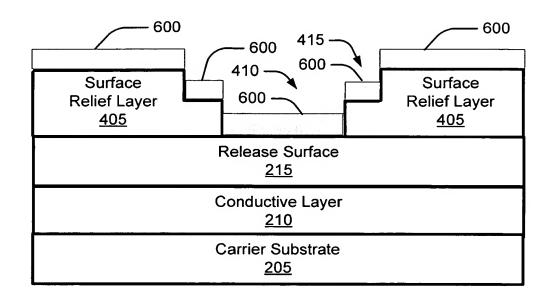
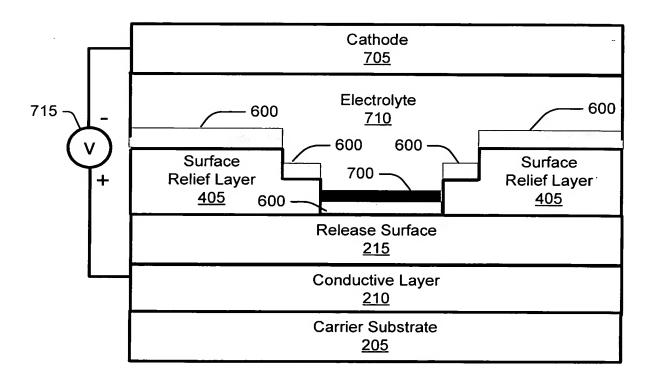


Fig. 6



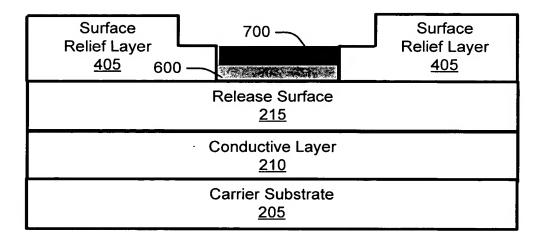


Fig. 8

700		
<u>405</u>	600	<u>405</u>
Release Surface 215		
Conductive Layer 210		
Carrier Substrate <u>205</u>		

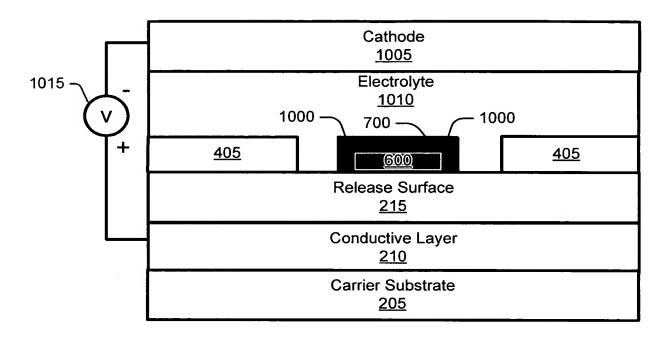
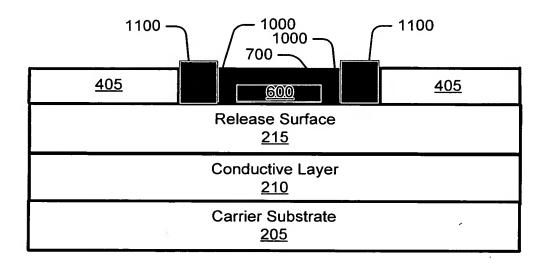
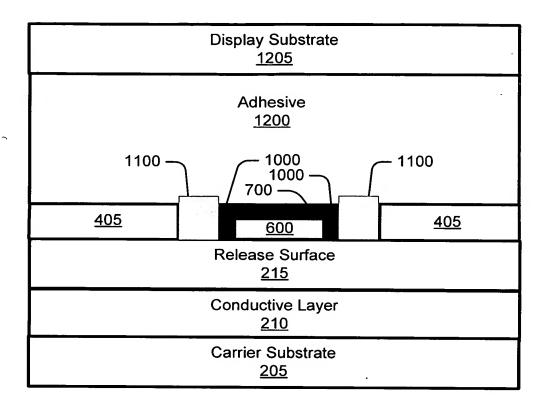
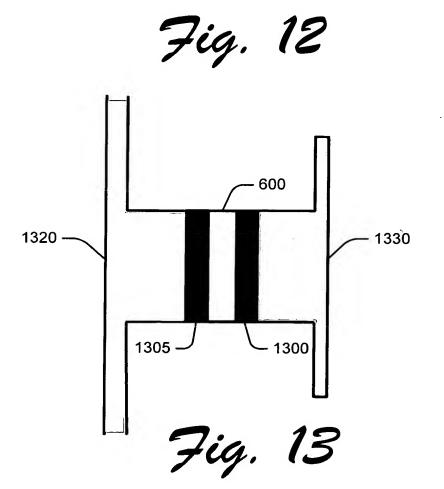


Fig. 10







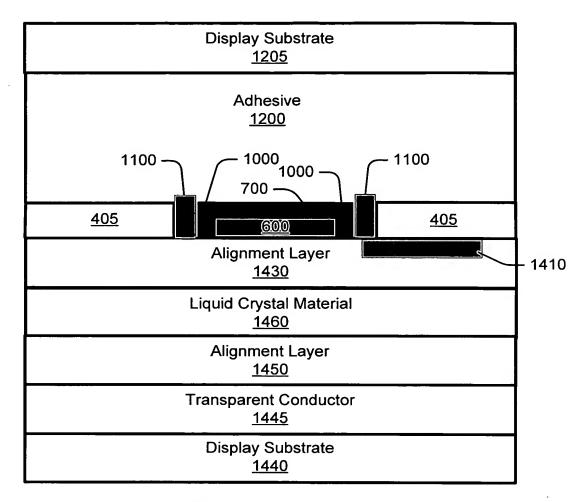
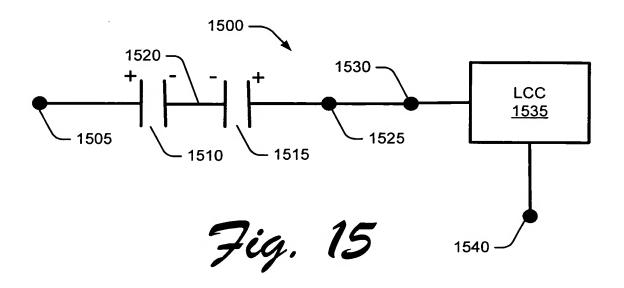


Fig. 14



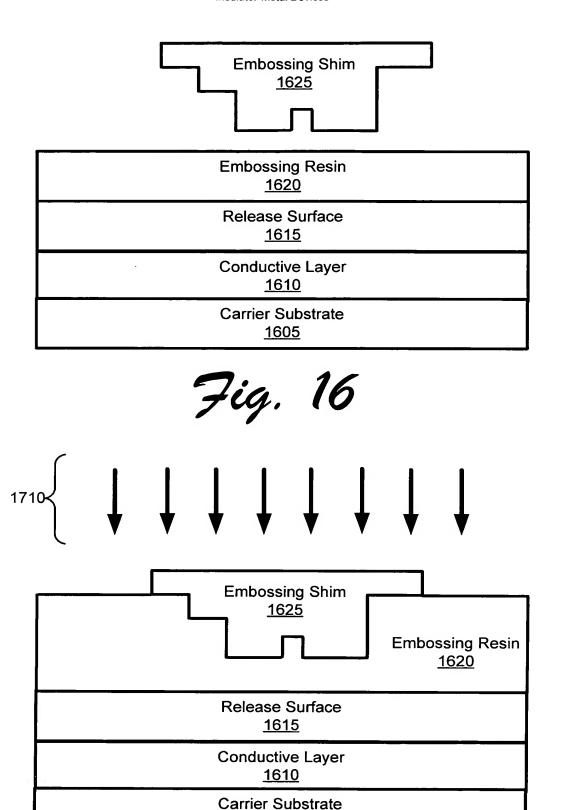


Fig. 17

<u>1605</u>

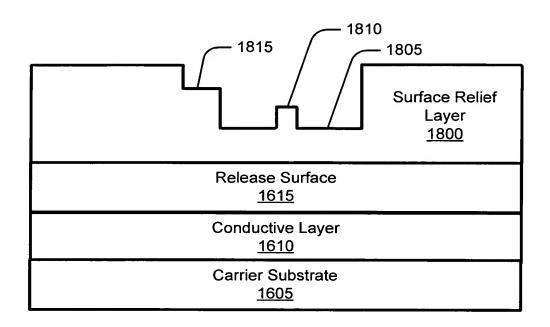
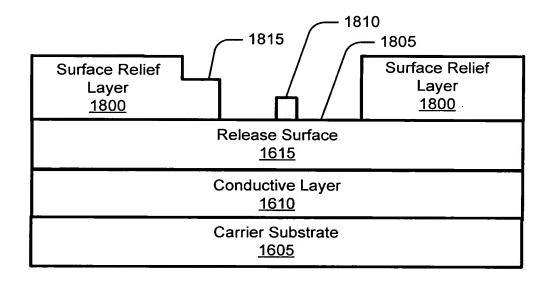


Fig. 18



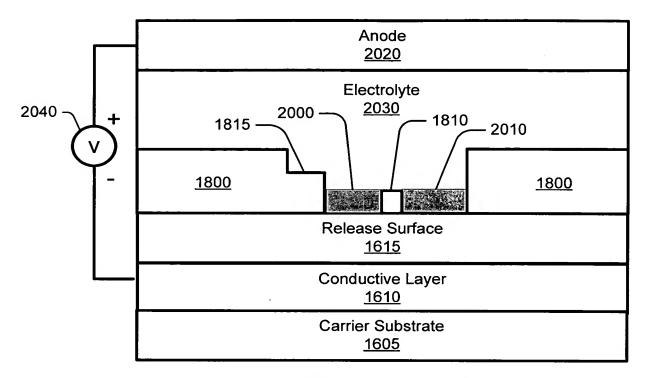
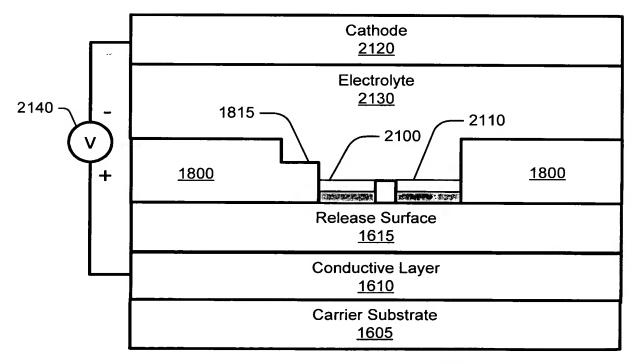


Fig. 20



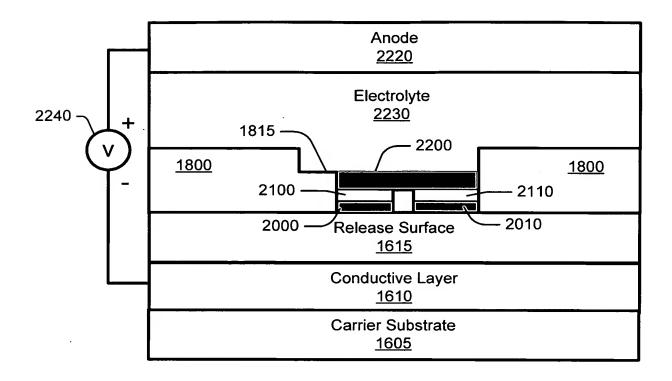
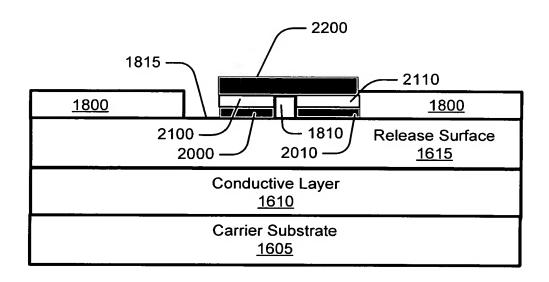


Fig. 22



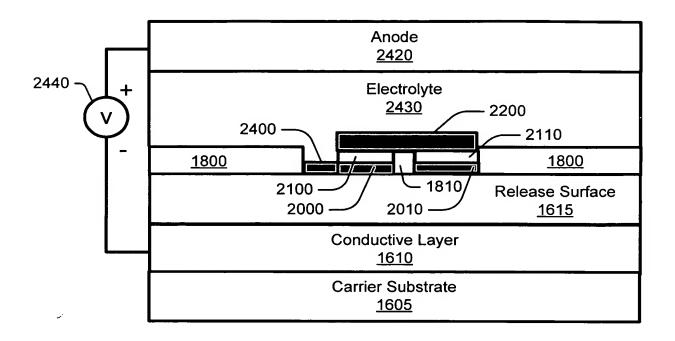


Fig. 24

